Remarks

Claims 1-15, and 25-28 are pending.

Claims 18-21 are cancelled.

Claims 16-17, and 22-24 are withdrawn.

Claims 14-15 have been amended.

Claims 25-28 are new.

The rejections are traversed.

Claim Amendments

Claims 14-15 have been amended and claims 25-28 are new. Support for the amendment and the new claims may be found in the application as filed, for example, on pages 2-4 and FIGs. 3-5. No new matter has been added.

Amendments to the Drawings

FIG. 4 has been amended to correct the labels of the data transition counters (DTC). Support for the amendment may be found in the specification as filed on pages 3 and 4. No new matter has been added.

Claim Rejections Under 35 USC §101

Claims 14-15 are rejected under 35 USC §101 because the claimed invention is directed to non-statutory subject matter.

Claims 14 and 15 have been amended to be directed towards an article of machine-readable code. Accordingly, claims 14 and 15 are now directed towards statutory subject matter under 35 U.S.C. 101.

Claim Rejections Under 35 USC §103

Claims 1-15 are rejected under 35 USC §103(a) as being unpatentable over various combinations of Halbert, et al., U.S. Patent Application Publication No. 2002/0112119 (hereinafter "Halbert"), Kim, U.S. Patent Application Publication No. 2003/0174544 (hereinafter

"Kim"), Little, et al., U.S. Patent No. 6,038,655 (hereinafter "Little"), Boggs, et al., U.S. Patent No. 5,530,696 (hereinafter "Boggs"), Bliss, et al., U.S. Patent Application Publication No. 2004/0056782, and the applicant's admitted prior art (AAPA).

Claim 5 includes at least one transition detection circuit configured to detect whether an achieved data transition density on at least one data lane is less than a desired data transition density for the at least one data lane. Thus, the achieved data transition density is compared against the desired data transition density. A desired data transition density indicates a preference for one data transition density over another. Claim 3 and claim 14 include a similar desired data transition density.

Claim 5 was rejected using the combination of Halbert and Kim. However, the combination of Halbert and Kim does not teach or suggest such a desired data transition density. The Examiner appears to be referring to the number of transitions N/2 of Kim as the desired data transition density. *Kim, ¶20-22.* However, in Kim, the number of transitions between a current parallel data and a previously input parallel data is used to generate corrected clock signals with delays dependent on the number of transitions. *Kim, ¶20-22, and 24-25.*

Although something happens in response to the number of transitions in Kim, no number of transitions is desired over another number of transitions. Thus, the number of transitions N/2 is at best a data transition density, not a desired data transition density as recited in claim 5. Furthermore, the addition of Halbert does not cure the deficiencies of Kim. There is no suggestion in the cited references of record or the knowledge of one skilled in the art to treat the number of transitions N/2 as a desired data transition density. The Applicant requests that the Examiner withdraw the rejections of claims 3, 5, 14, and dependent claims 6-13, and 15.

Claim 1 includes transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density. Claim 1 was rejected using the combination of Halbert and Kim. However, the combination of Halbert and Kim does not teach or suggest transmitting such a synchronization signal.

The clock signal CLK is delayed into clock signals mCLK and mCLKb according to the control signal CTRL which was generated according to the number of transitions of the parallel data. *Kim, ¶20-25.* These clock signals mCLK and mCLKb are not transmitted by the output driving part of Kim, only buffered data y0-y7 are transmitted. *Kim, ¶26.* Since, the delayed clock signals mCLK and mCLKb are not transmitted, the delayed clock signals mCLK and

mCLKb cannot be the synchronization signal of claim 1. There is no suggestion in the cited references of record or the knowledge of one skilled in the art to transmit the clock signals as a synchronization signal. The Applicant requests that the Examiner withdraw the rejections of claims 1 and dependent claims 2-4.

Claim 25 includes transmitting the synchronization signal having a number of transitions such that the achieved data transition density for the at least one data lane is greater than or equal to a desired data transition density. Thus, the synchronization signal causes the achieved data transition density to be greater than or equal to a desired data transition density.

Even if the clock signals mCLK and mCLKb or any resulting effect are interpreted as a synchronization signal, as described above, the data is merely retimed with the clock signals mCLK and mCLKb to reduce skew. The number of data transitions is not changed in response, only the timing of the data transitions. Thus, that signal does not affect the achieved data transition density. There is no suggestion in the cited references of record or the knowledge of one skilled in the art to transmit such a synchronization signal. The Applicant asserts that claim 25 is allowable of the cited references of record.

Claim 26 includes a transition detection circuit configured to detect whether an achieved transition density on a corresponding one of the at least one data lane is less than the desired data transition density for the corresponding data lane. The achieved transition density is specific to a single data lane.

As described above Kim examines the transitions from currently input parallel data to previously input parallel data. The cited desired transition density is the number of transitions for all of the lines of the parallel data. Thus, any achieved transition density is the achieved transition density over multiple data lines, not a corresponding one data lane.

Boggs does disclose a transition counter for counting transitions of a data input signal. *Boggs, col. 6, ll. 22-23.* However, Boggs does not suggest a desired data transition density. In addition, as the Examiner combined Boggs with Kim, the transition counter is on each line of the parallel data lines in Kim. If the outputs of the transition counters are combined, it is an achieved data transition density of multiple data lines that is compared with the N/2 transition density of Kim. Such an achieved data transition density is not an achieved data transition density of a corresponding one data lane.

In the event that the parallel data is interpreted by the Examiner as a single data lane, claim 27 further refines claim 26 in that the corresponding data lane is a serial data lane. Thus, the parallel data lines of Kim cannot be the serial data lane of claim 27.

There is no suggestion in the cited reference of record or the knowledge of one skilled in the art to detect such an achieved data transition density on one data lane. The Applicant asserts that claims 26 and 27 are allowable of the cited references of record.

Claim 28 includes a time period that is greater than two clock cycles. Claim 8, the parent claims of claim 28, includes a logic block configured to signal when at least one of the plurality of data transition counters counts, during a time period defined by the clock cycle counter, a number of data transitions detected by the corresponding data transition detector that is less than the desired data transition density. Thus, the data transition counters count for longer than two clock cycles.

As described above, Boggs discloses a transition counter. The transition counters are cleared after each timer period. *Boggs, col. 6, ll. 42-47.* The timer period may be defined by 977 transitions of an 8 MHz clock. *Boggs, col. 6, ll. 15-21.*

However, counting transitions for such a time period is in direct conflict with the solution of Kim. In Kim, an amount of skew on output lines is introduced based on the pattern of the parallel output data. *Kim, ¶4.* This skew is introduced into the parallel data as it is being output. To compensate for this skew in Kim, when the pattern changes as indicated by the number of transitions, a clock used to retime the parallel data prior to being output is delayed to compensate for the expected skew on the output. The amount of delay is specific to that set of simultaneously output parallel data. An earlier or later set of parallel data may have a completely different number of transitions, resulting in a completely different skew.

If the data transition density is counted over more than two clock cycles as recited in claim 28, the delay for the clock will be offset from the parallel data generating the transitions by more than two clock cycles. The compensating delay will no longer be synchronized with the parallel data needing the compensating delay. In fact, the compensating delay may be applied to a set of parallel data needing an delay in the opposite direction, increasing the output skew. As a result, the improvement resulting from Kim will be eliminated and the problem may be exaggerated by counting the transitions over multiple clock cycles.

The Applicant asserts that claim 28 is allowable of the cited references of record.

For the foregoing reasons, reconsideration and allowance of claims 1-28 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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CLAIMS AS AMENDED					
For:	Number After Amendment	Previous Number	Extra	Rate	Additional Fee
Total Claims	24	24	0	x $50 =	$ 0
Independent Claims	5	6	0	x $200 =	$ 0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					$ 0

Any deficiency or overpayment should be charged or credited to deposit acct. no. 13-1703.